



CAMOSUN COLLEGE
School of Trades & Technology
Electronics & Computer Engineering Department

ECET 231
CAD FOR ELECTRONICS
Winter 2020

COURSE OUTLINE

The calendar description is available on the web @

www.camosun.ca

Ω Please note: This outline will not be kept indefinitely. It is recommended students keep this outline for their records, especially to assist in transfer credit to post-secondary institutions.

CALENDAR DESCRIPTION

This course introduces Altium Designer 17 (or later edition), a computer-based electronics design software for engineers/technologists to design printed circuit boards (PCB), FPGA, and embedded software, and to manage project data. Students learn how to create the electronic schematic of a circuit, how to use schematic libraries to select and design electronic components, and how to plan a printed circuit board layout. Students use these skills to create a printed circuit board from a schematic diagram.

1. Instructor Information

(a) Instructor	JOHN J. YANG
(b) Office hours	TBD
(c) Location	TEC 268
(d) Phone	(250) 370-4213 Alternative: _____
(e) E-mail	yang@camosun.bc.ca
(f) Website	http://camosun.ca/learn/programs/electronics-computer-engineering-technolog

2. Intended Learning Outcomes

(If any changes are made to this part, then the Approved Course Description must also be changed and sent through the approval process.)

OBJECTIVES

- Be able to draw schematic diagrams (simple/parallel/hierarchical)
- Be able to find, select, and create schematic components (schematic library editor)
- Be able to lay out multi-layer printed circuit boards (PCB)
- Be able to find, select, and create PCB footprints (PCB library editor)
- Be able to create 3D view of a PCB
- Be able to manage the PCB project data

3. Required Materials

(a) Texts

ECET 231 Course Notes

(b) Other

Altium websites (www.altium.com)

4. Course Content and Schedule

(Can include: Class hours, Lab hours, Out of Class Requirements and/or Dates for quizzes, exams, lecture, labs, seminars, practicums, etc.)

CREDIT 2.0
IN-CLASS WORKLOAD: 3 hours / week
OUT-OF-CLASS WORKLOAD: 3 hours / week
PREREQUISITES ECET 242, 260

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TABLE OF CONTENTS

SECTION I – The Basics of Altium Designer 19	Week 1
§1 Introduction to Altium Designer 19	
§1.1 Review of schematic circuits and printed circuit boards	
§1.2 Introduction to the environment of Altium	
§1.3 A simple schematic circuit capture – Lab01	
§2 Schematic capture editor	Week 2
§2.1 Elements and tools of the schematic capture editor	
§2.2 10-step procedure of creating schematic captures	
§2.3 How to find desired schematic components (symbols)	
§2.4 How to install proper (schematic) libraries	
§2.5 Electrical rules setting -- for schematic captures	
§2.6 Netlist and bill of materials (BOM)	
§2.7 Project library versus general library	
§2.8 Troubleshoot schematic captures	
§2.9 A de-morgenized logic circuit capture – Lab02	
§3 PCB layout editor	Week 3-4
§3.1 Elements and tools of the PCB layout editor	
§3.2 10-step procedure of creating PCB layouts	
§3.3 PCB document wizard	
§3.4 How to find desired PCB components (footprints)	
§3.5 How to install proper (PCB) libraries	
§3.6 Import (netlist) changes versus Update PCB	
§3.7 Design rules setting -- for PCB layouts	
§3.8 Manual route versus auto route	
§3.9 Troubleshoot a PCB layout	
§3.10 Reshape a PCB board (re-size)	

- §3.11 How to pour polygon
- §3.12 Fabrication outputs versus assembly outputs
- §3.13 A through-hole single-sided PCB design – Lab03-04

SECTION II – Library Editors _____ Week 5

- §4 Schematic Library Editor
- §4.1 What is the schematic library editor?
- §4.2 Elements and tools of the schematic library editor
- §4.3 Three ways to create a schematic component (electrical symbol) – Lab05

§5 PCB Library Editor _____ Week 6

- §5.1 What is PCB library editor?
- §5.2 Elements and tools of the PCB library editor
- §5.3 Three ways to create a PCB footprint (PCB symbol) – Lab06

SECTION III – Advanced Designs, Considerations, and Data Management _____ Week 8-12

- §6 PCB with multiple signal layers & multiple internal planes
- §6.1 Parallel format of a multi-channel schematic capture
- §6.2 Hierarchical format of a multi-channel schematic capture – Lab07-08
- §6.3 PCB layout with two signal layers (double sided)
- §6.4 PCB layout with two signal layers and two internal planes (power/ground)
- §6.5 Split internal planes – Lab09-10
- §6.6 PCB layout with more than two signal layers and/or two internal planes
- §6.7 Layer stack management

§7. The advanced knowledge of PCB and Altium Designer 19 _____ Week 13-14

- §7.1 Schematic template management
- §7.2 Board layers and Colors management (PCB)
- §7.3 Track width management
- §7.4 Holes and vias management
- §7.5 Solder paste/mask management
- §7.6 Room & Classes management
- §7.7 Mechanical layers management
- §7.8 3-D model management – Lab11
- §7.9 Grounding and de-coupling
- §7.10 EMI/EMC considerations
- §7.11 High speed signal considerations
- §7.12 Thermal Analysis – Lab12* (* when time is allowed)
- §7.13 Differential pair & length matching
- §7.14 BGA components layout – Lab13* (* when time is allowed)
- §7.15 PCB project management

Appendix: Protel 2004/DXP shortcut keys

Labs

- Lab #1 Introduction to Altium Designer 19
- Lab #2 Simple logic Circuit Schematic Capture
- Lab #3-4 Single-sided PCB Layout
- Lab #5 Schematic Library Editor – create schematic symbols
- Lab #6 PCB Library Editor – create PCB footprints

Lab #7-8 Multi-sheet Schematic Design
Lab #9-10 Multi-layer PCB Design
Lab #11 3D PCB Design
Lab #12* Optimized PCB Power Distribution Network (PDN)
Lab #13* BGA PCB Design

(* when time is allowed)

5. Basis of Student Assessment (Weighting)

(Should be directly linked to learning outcomes.)

- (a) Assignments

- (b) Quizzes

- (c) Exams

- (d) Other (e.g. Project, Attendance, Group Work)

EVALUATION* [* Delay levy (labs/assignments): -10% per day]

Attendance to all classes and satisfactory completion of all assignments and labs are mandatory. The lab grade, the theory grade, and the final exam must be over 50% to pass the course. The final grade will be determined by the following components:

- Lab exercises (13) 50%
- Midterm Exam 20%
- Final Exam 30%
- Grading: in accordance with Camosun College Policy

6. Grading System

(If any changes are made to this part, then the Approved Course description must also be changed and sent through the approval process.)

(Mark with "X" in box below to show appropriate approved grading system – see last page of this template.)

- Standard Grading System (GPA)
- Competency Based Grading System

7. Recommended Materials to Assist Students to Succeed Throughout the Course

8. College Supports, Services and Policies



Immediate, Urgent, or Emergency Support

If you or someone you know requires immediate, urgent, or emergency support (e.g. illness, injury, thoughts of suicide, sexual assault, etc.), **SEEK HELP**. Resource contacts @

<http://camosun.ca/about/mental-health/emergency.html> or <http://camosun.ca/services/sexual-violence/get-support.html#urgent>

College Services

Camosun offers a variety of health and academic support services, including counselling, dental, disability resource centre, help centre, learning skills, sexual violence support & education, library, and writing centre. For more information on each of these services, visit the **STUDENT SERVICES** link on the College website at <http://camosun.ca/>

College Policies

Camosun strives to provide clear, transparent, and easily accessible policies that exemplify the college's commitment to life-changing learning. It is the student's responsibility to become familiar with the content of College policies. Policies are available on the College website at <http://camosun.ca/about/policies/>. Education and academic policies include, but are not limited to, Academic Progress, Admission, Course Withdrawals, Standards for Awarding Credentials, Involuntary Health and Safety Leave of Absence, Prior Learning Assessment, Medical/Compassionate Withdrawal, Sexual Violence and Misconduct, Student Ancillary Fees, Student Appeals, Student Conduct, and Student Penalties and Fines.

A. GRADING SYSTEMS <http://www.camosun.bc.ca/policies/policies.php>

The following two grading systems are used at Camosun College:

1. Standard Grading System (GPA)

Percentage	Grade	Description	Grade Point Equivalency
90-100	A+		9
85-89	A		8
80-84	A-		7
77-79	B+		6
73-76	B		5
70-72	B-		4
65-69	C+		3
60-64	C		2
50-59	D		1
0-49	F	Minimum level has not been achieved.	0

2. Competency Based Grading System (Non GPA)

This grading system is based on satisfactory acquisition of defined skills or successful completion of the course learning outcomes

Grade	Description
COM	The student has met the goals, criteria, or competencies established for this course, practicum or field placement.

DST	The student has met and exceeded, above and beyond expectation, the goals, criteria, or competencies established for this course, practicum or field placement.
NC	The student has not met the goals, criteria or competencies established for this course, practicum or field placement.

B. Temporary Grades

Temporary grades are assigned for specific circumstances and will convert to a final grade according to the grading scheme being used in the course. See Grading Policy at <http://www.camosun.bc.ca/policies/E-1.5.pdf> for information on conversion to final grades, and for additional information on student record and transcript notations.

Temporary Grade	Description
I	<i>Incomplete:</i> A temporary grade assigned when the requirements of a course have not yet been completed due to hardship or extenuating circumstances, such as illness or death in the family.
IP	<i>In progress:</i> A temporary grade assigned for courses that are designed to have an anticipated enrollment that extends beyond one term. No more than two IP grades will be assigned for the same course.
CW	<i>Compulsory Withdrawal:</i> A temporary grade assigned by a Dean when an instructor, after documenting the prescriptive strategies applied and consulting with peers, deems that a student is unsafe to self or others and must be removed from the lab, practicum, worksite, or field placement.