CAMOSUN COLLEGE

Department of Electronics

ECET 162 Digital Electronics 2

Hours: 3/2/0

Prerequisite: ECET 161 Digital Electronics 1

Short description:
Students will study sequential logic, the implementation of digital circuits using advanced programmable logic devices, counters and shift registers, state machine design, logic gate circuits and the interfacing of analog and digital circuits. Students learn how to construct a simple computer from basic computing elements.

Learning outcomes:
Upon successful completion of this course, students will be able to:

- describe the features of sequential systems;
- design sequential circuits;
- use an integrated development environment (IDE) to develop and program digital circuits;
- program counters and shift registers in Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL);
- design and implement state machines in advanced programmable logic devices;
- describe electric characteristics and interfacing requirements of digital components;
- design interfaces to digital circuits using field programmable gate arrays(FPGAs);
- explain the differences between memory systems;
- describe key elements of microprocessor architecture;
- follow prescribed safety procedures appropriate to an electronics laboratory.

Course outline:

1. Introduction to sequential logic **5 hours**
- 1.1 Latches
- 1.2 NAND/NOR latches
- 1.3 Gated latches
- 1.4 Edge-triggered D flip-flops
- 1.5 Edge-triggered JK flip-flops
- 1.6 Edge-triggered T flip-flops
- 1.7 Timing parameters

2. Introduction to programmable logic architectures **5 hours**
- 2.1 Programmable sum-of-products arrays
- 2.2 PAL fuse matrix and combinatorial outputs
- 2.3 PAL outputs with programmable polarity
- 2.4 PAL devices with programmable polarity

2.5 Universal PAL and generic array logic
2.6 Complex programmable logic devices (CPLDs)
2.7 Field programmable logic arrays (FPGAs)

3. Counters and shift registers **6 hours**
3.1 Basic concepts of digital counters
3.2 Synchronous counters
3.3 Design of synchronous counters
3.4 Programming binary counters in VHDL
3.5 Control options for synchronous counters
3.6 Programming presettable and bidirectional counters in VHDL
3.7 Shift registers
3.8 Programming shift registers in VHDL
3.9 Shift register counters

4. State machine design **7 hours**
4.1 State machines
4.2 State machines with no control inputs
4.3 State machines with control inputs
4.4 Switch de-bouncer for a normally open pushbutton switch
4.5 Unused states in state machines
4.6 Traffic light controller

5. Logic gate circuits **3 hours**
5.1 Electrical characteristics of logic gates
5.2 Propagation delay
5.3 Fanout
5.4 Power dissipation
5.5 Noise margin
5.6 Interfacing TTL and CMOS gates
5.7 Internal circuitry of TTL gates
5.8 Internal circuitry of CMOS gates
5.9 TTL and CMOS variations

6. Interfacing analog and digital circuits **4 hours**
6.1 Analog and digital signals
6.2 Digital-to-analog conversion
6.3 Analog-to-digital conversion
6.4 Data acquisition

7. Memory devices and systems **3 hours**
7.1 Basic memory concepts
7.2 Random access read/write memory (RAM)
7.3 Read only memory (ROM)
7.4 Sequential memory: FIFO and LIFO
7.5 Dynamic RAM modules

8. Microprocessor architecture **4 hours**
8.1 Registers
8.2 Program counter

8.3	Instruction set and decoder
8.4	Arithmetic logic unit (ALU)
8.5	State machines timing and control
8.6	Address, data and control buses
8.7	Memory systems

Tests and review	5 hours
Total	**42 hours**

Textbooks (Optional):

- "Digital Design with CPLD Applications and VHDL 2nd ed.", Robert K. Dueck
- "Digital Electronics: A Practical Approach with VHDL, 9th Edition", William Kleitz

Video:

- Youtube has video for the "Digital Electronics: A Practical Approach with VHDL, 9th Edition" on the authors channel: billkleitz
  https://www.youtube.com/channel/UCFC56lANq_FESHes9j0NKnw

Marks:

Lecture:	Term Test(s)	35
	Final Exam	40
	Total Lecture Marks.....	75
Lab:	Preparation/completion	25
	Total Lab Marks.....	25
	TOTAL.....	100

NOTE:
The marks awarded in the lab are for lab performance, preparation of exercises and for completion of exercises on time. Late labs will be graded out of 50% of the original mark. **The student will be required to re-do all or part of any exercise deemed unsatisfactory until a satisfactory level is achieved.**

A minimum grade of "C" is required in order to continue on to courses for which this is a pre-requisite. To obtain at least a C grade:

- The student must obtain a composite mark of **at least 60%**.
- ALL lab exercises must be completed **to a "satisfactory" level. Failure to do so in a timely* manner will result in a grade of "F" for the course.** ***(*Absolute deadline for completion of all lab exercises will be announced.)***