

CAMOSUN COLLEGE  
**ELECTRONICS ENGINEERING DEPARTMENT**

**(ECET 280)**

COURSE OUTLINE

Instructor: Mozhgan Bacon  
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**CALENDAR DESCRIPTION**

**ECET 280 Data Acquisition & Programmable Logic Controllers**

This course offers a comprehensive study of data acquisition (DAQ) systems including: sampling theory, aliasing, time and frequency domains representation, anti-aliasing and recovery filter design, sample-and-hold (S/H) techniques, quantization theory, analog-to-digital (A/D) and digital-to-analog (D/A) converters, and the virtual instrumentation software LabVIEW. This course also covers major topics of programmable logic controllers (PLCs) including: PLC addressing and basic instructions, PLC Ladder logic, PLC timer and counter functions, PLC comparison and math operations, data handling and program flow control.

OFFERED:	Semester 3 (fall)
CREDIT:	3
IN-CLASS WORKLOAD:	3 lecture, 2.5 lab /week
OUT-OF-CLASS WORKLOAD:	6 hours /week
PREREQUISITES:	ECET 165

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**OBJECTIVE**

- Be able to critique Data Acquisition (DAQ) systems in following aspects: signal acquiring, signal conditioning, and signal digitizing.
- Be able to use programmable logic controllers (PLCs)
- Be able to program the virtual instrumentation software LabVIEW

## TABLE OF CONTENTS

### **Part I      Data Acquisition Systems**

- 1. Introduction to Data Acquisition (DAQ) systems** **2 hours**
  - 1.1. DAQ, DDS and “pure” computer systems
  - 1.2. Five stages of a DAQ system
  - 1.3. Relationships between stages
  - 1.4. DSP applications in DAQ systems
  
- 2. Signal Conditioning and sample-hold circuits** **8 hours**
  - 2.1. Introduction to Signal Conditioning
  - 2.2. Anti-aliasing and reconstruction filters
  - 2.3. Switched capacitor filters
  - 2.4. Sampling theory
  - 2.5. Sample-hold circuit design
  
- 3. Analog-to-Digital (A/D) converters and Digital-to-Analog (D/A) converters** **8 hours**
  - 3.1. Quantization theory
  - 3.2. Digital-to-analog (D/A) converters
  - 3.3. Analog-to-digital (A/D) converters
  - 3.4. The frequency relationship between A/D converters and S/H circuits
  - 3.5. A/D and D/A circuits design
  - 3.6. Voltage-to-frequency (V/F) and frequency-to-voltage (F/V) converters
  
- 4. Instrumentation** (*selective*) **6 hours**
  - 4.1. Review of transducers and signal conditioning
  - 4.2. Voltage references
  - 4.3. Analog multiplexers and demultiplexers
  - 4.4. Field wiring: shielding, grounding and noise considerations
  - 4.5. Errors in data acquisition systems
  - 4.6. DAQ systems specification
  - 4.7. Examples of DAQ systems design
  - 4.8. Over-sampling versus under-sampling

### **Part II      Laboratory Virtual Instrument Engineering Workbench (LabVIEW)**

- 5. Introduction to LabVIEW** (*to be done in the lab*) **2 hours**
  - 5.1. What is LabVIEW
  - 5.2. LabVIEW control panels, block diagrams, and tools
  - 5.3. LabVIEW functions and subroutines (sub-vi)
  - 5.4. LabVIEW Serial communication and network communication

## **Part III Programmable Logic Controllers (PLCs)**

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| <b>6. Introduction to PLCs</b>                       | <b>2 hours</b> |
| 6.1. What are PLCs                                   |                |
| 6.2. Input/output devices                            |                |
| 6.3. PLC hardware – Allen-Bradley controllers        |                |
| 6.4. PLC software – LogixPro 500 and RSLogix 500     |                |
| <b>7. PLC addressing and basic instructions</b>      | <b>2 hours</b> |
| 7.1. Allen-Bradley PLC addressing                    |                |
| 7.2. Basic input/output instructions                 |                |
| 7.3. Branches  |                |
| <b>8. Ladder logic programming</b>                   | <b>4 hours</b> |
| 8.1. Boolean statements and Ladder logic equivalents |                |
| 8.2. Commonly used ladder logic sequences            |                |
| 8.3. Properly formatted outputs                      |                |
| 8.4. Boolean logic and truth table review            |                |
| <b>9. PLC functions and operations</b>               | <b>8 hours</b> |
| 9.1. Timers  |                |
| 9.2. Counters  |                |
| 9.3. Math instructions                               |                |
| 9.4. Comparison                                      |                |
| 9.5. Data handling                                   |                |
| 9.6. Program flow control                            |                |
| 9.7. Bit shifts and Sequencer                        |                |

### **TEXTBOOKS AND REFERENCES**

1. Max Rabiee, **Programmable Logic Controllers: Hardware and Programming**, 3<sup>rd</sup> Edition, G-W Publisher, ISBN: 978-1-60525-945-1
2. James A. Rehg, Glenn J. Sartori: **Programmable Logic Controllers**, 2<sup>nd</sup> Edition, Pearson Education Limited, ISBN: 978-0-13-504881-8
3. ECET 280 Course Notes
4. Instructor's handouts
5. Manufacturers' datasheets

## **LABORATORIES**

1. LabVIEW (I) – Introduction to LabVIEW
2. LabVIEW (II) – Functions and Sub-VI
3. LabVIEW (III) – DataSocket and Serial Communication
4. Anti-aliasing filter
5. Sample-and-hold circuit
6. Digital-to-analog converter
7. Analog-to-digital converter
8. PLCs (I) – Introduction to LogixPro 500 PLC Simulator
9. PLCs (II) – Garage Door Control
10. PLCs (III) – Silo system
11. PLCs (IV) – Traffic control
12. PLCs (V) – Introduction to Allen-Bradley PLCs and RSLogix 500
13. PLCs (VI) – Analog I/O modules (MicroLogix 1200)
14. PLCs (VII) – PWM/PID control (MicroLogix 1200)

## **EVALUATION**

- Labs 20%
- Assignments and Quizzes 20%
- Midterm Exam 20%
- Final Exam 40%

## **GRADING** In accordance with College policy

### **Letter Grades:**

<b>A+</b>	90 – 100%	<b>B-</b>	70 - 72%
<b>A</b>	85 - 89%	<b>C+</b>	65 – 69%
<b>A-</b>	80 - 84%	<b>C</b>	60 - 64%
<b>B+</b>	77 - 79%	<b>D</b>	50 - 59%
<b>B</b>	73 - 76%	<b>F</b>	0 - 49%

**A minimum of 50% must be achieved in each of the theory and lab portions to pass the course.** Less than 50% in either portion will result in a failure of the entire course.

## ECET 280 course outline

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Note:

- Lab and lecture portions **MUST** be passed individually.
- Late penalties of 10% per day will be applied at the instructor's discretion.
- Lab attendance is **MANDATORY**. Failure to attend sufficient labs will result in an F grade.
- Lab grades will not be awarded for missed labs without a valid reason for absence.