ECET 161 Digital Electronics 1

Hours: 3/2/0

Prerequisite: C+ in Principles of Math 12 or Pre-calculus 12, or C in Calculus 12 and Pre-calculus 12, or C in Calculus 12 and Principles of Math 12, or C+ in MATH 093, or C in MATH 105, or C+ in MATH 107, or C in MATH 115, or C in MATH 173, or assessment; C in Physics 11 or PHYS 101 or PHYS 151; C in English 12 or English First Peoples 12 or TPC 12, or in ENGL 092 and ENGL 094, or in ENGL 092 and ENGL 096, or in ENGL 103 and ENGL 104, or in ENGL 103 and ENGL 106, or in ENGL 130, or in ENGL 142, or in ELD 092 and ELD 094, or in ELD 097, or assessment

Pre/corequisite: ECET 140 Electronic Circuit Fundamentals

Short description:
Students will be provided with an introduction to digital technology, using discrete logic gates and advanced programmable logic devices. They will learn basic digital concepts as well as the design of combinatorial digital circuits.

Learning outcomes:
Upon successful completion of this course a student will be able to:

- explain the difference between analog and digital systems;
- describe the features of combinatorial systems;
- perform numerical operations using decimal, binary and hexadecimal number systems;
- identify gates in digital schematics;
- explain the basic operation of a logic gate;
- recognize digital logic symbols and use them to draw digital circuits;
- use algebraic forms and truth tables to express circuit function;
- design combinatorial circuits;
- explain multiplexing and de-multiplexing operations;
- explain the operation of digital arithmetic circuits;
- program an advanced programmable logic device using design software;
- determine logic levels in practical digital circuits;
- use appropriate test equipment to troubleshoot digital circuits.

Textbooks (Optional):

- “Digital Design with CPLD Applications and VHDL 2nd ed.”, Robert K. Dueck
- "Digital Electronics: A Practical Approach with VHDL, 9th Edition", William Kleitz

Video:

- Youtube has video for the “Digital Electronics: A Practical Approach with VHDL, 9th Edition” on the authors channel: billkleitz
  https://www.youtube.com/channel/UCFC56lANq_FESHes9j0NKnw

Evaluation:

Lecture:	Term Test(s)	25
	Final Exam	35
	Total Lecture Marks.....	60
Lab:	Preparation/completion	40
	Total Lab Marks.....	40
	TOTAL.....	100

NOTE:
The marks awarded in the lab are for lab performance, preparation of exercises and for completion of exercises on time.
A minimum grade of "C" is required in order to continue on to courses for which this is a pre-requisite. To obtain at least a C grade:

- The student must obtain a composite mark of **at least 60%**.
- Late labs will be graded out of 50% of the original mark.
- ALL lab exercises must be completed **to a "satisfactory" level. Failure to do so in a timely* manner will result in a grade of "F" for the course.** ***(*Absolute deadline for completion of all lab exercises will be announced.)***

Course outline:

1. Introduction to digital systems **1 hour**

- 1.1 Analog versus digital
- 1.2 Deductive logic
- 1.3 Combinatorial versus sequential

2. Describing combinatorial logic systems **1 hour**

- 2.1 Decimal number system
- 2.2 Binary number system
- 2.3 Hexadecimal number system
- 2.4 BCD code
- 2.5 Logic variable combinations
- 2.6 The truth table

3. Logic signals **2 hours**

- 3.1 Logic voltage levels
- 3.2 Simple resistor-LED circuit[1]
- 3.3 Variable names, signal names and active levels
- 3.4 Active levels for pins
- 3.5 The state indicator
- 3.6 The logic probe
- 3.7 Providing logic levels with switches

4. Logic operations and gates **4 hours**

- 4.1 Basic logic operations
- 4.2 Logic symbols for real devices
- 4.3 Naming gates
- 4.4 Gate duality

4.5 Introduction to digital ICs
4.6 LEDs as logic indicators
4.7 Hardware options
4.8 Truth tables versus function tables

5. Analysis of combinatorial circuits **4 hours**

5.1 Evaluating circuit outputs
5.2 Describing logic circuits algebraically
5.3 Boolean theorems
5.4 The Boolean Sum-of-Products (SOP) form
5.5 Truth tables from expressions
5.6 Redrawing circuits using gate duality
5.7 Faultfinding in combinatorial circuits

6. Logic circuit design **6 hours**

6.1 Common circuit configurations
6.2 Developing output expressions directly
6.3 Hardware implementation of Boolean expressions
6.4 Deriving expressions from a truth table
6.5 Minimization of Boolean expressions
6.6 Applying “don’t care” input conditions
6.7 Summary of logic design steps
6.8 Logic design example

7. CPLDs and FPGAs **6 hours**

7.1 What are CPLDs and FPGAs?
7.2 Programming CPLDs and FPGAs using Quartus II
7.3 Graphic design file
7.4 Compiling Quartus II files
7.5 Hierarchical design
7.6 Text design file (VHDL)
7.7 Creating a physical design

8. Combinatorial logic applications **6 hours**

8.1 Encoders and decoders
8.2 Multiplexers
8.3 Demultiplexers
8.4 Multiplexed displays
8.5 Tristate and open collector logic
8.6 Parity generators and checkers

9. Digital arithmetic circuits **7 hours**

9.1 Digital arithmetic
9.2 Representing signed binary numbers
9.3 Signed binary arithmetic
9.4 Hexadecimal arithmetic
9.5 Numeric and alphanumeric codes
9.6 Binary adders and subtractors
9.7 BCD adders
9.8 Carry generation in Quartus II

Tests and review 5 hours
Total **42 hours**

Labs:

1. Number systems and truth tables
2. Logic levels
3. Logic gates and gate duality
4. Boolean algebra and logic circuits
5. Setup and testing or construction of microcontroller board
6. VHDL or graphical design in Quartus II
7. Decoder design in VHDL
8. Multiplexer design in VHDL
9. Time division multiplexer and demultiplexer design
10. 4-bit parallel adder design
11.
12.
13.
14.