CAMOSUN COLLEGE

TWR:01/14

Department of Electronics Rev 1.0

ELEN 164 DIGITAL LOGIC

Instructor:	James van Oort	Office:	TEC269
Lecture:	3 hrs/wk	Email:	vanoort@camosun.bc.ca
Lab:	2 hrs/wk		

Textbooks:

- "ELEX 164 Digital Logic",
  Camosun College, Latest revision.
- "TTL Logic Data Book",
  Texas Instruments, Latest edition
- **(optional)** Tocci, Ronald J.,
  "Digital Systems principles and applications",
  Prentice-Hall Inc., Sixth Edition, 1995.

Evaluation:

Lecture:	Quizzes and Assignments	15
	Term Tests	30
	Final Exam	45
	Total Lecture Marks.....	90
Lab:	Preparation/completion	10
	Total Lab Marks.....	10
	TOTAL.....	100

NOTE:
The marks awarded in the lab are for preparation of exercises and for completion of exercises on time. Apart from this, numerical marks will not be assigned for lab work. Instead, lab exercises will be marked as "satisfactory" or "unsatisfactory". **The student will be required to re-do all or part of any exercise deemed unsatisfactory until a satisfactory level is achieved.**

A minimum grade of "C" is required in order to continue on to courses for which this is a pre-requisite. To obtain at least a C grade:

- The student must obtain a composite mark of **at least 60%**.
- ALL lab exercises must be completed **to a "satisfactory" level. Failure to do so in a timely* manner will result in a grade of "F" for the course.** ***(*Absolute deadline for completion of all lab exercises will be announced.)***
- All labs must be completed satisfactorily before the final exam to pass the course

LECTURE TOPICS

1. Introduction to Digital Systems (1/2 hr)
   - 1.1 Analog vs Digital
   - 1.2 Deductive Logic
   - 1.3 Combinatorial vs Sequential Logic Circuits

2. Describing Combinatorial Logic Systems (1-1/2 hrs)
   - 2.1 Decimal Numbers: Counting/Positional Weighting
   - 2.2 The Binary Number System
     - 2.2.1 Counting and Positional Weighting
     - 2.2.2 Binary/Decimal Conversions
   - 2.3 Logic Variable Combinations
   - 2.4 The Truth Table

3. Logic Signals (2 hrs)
   - 3.1 Logic Voltage Levels
   - 3.2 Variable Names, Signal Names and Active Levels
   - 3.3 Active Levels for Pins
   - 3.4 The State Indicator
   - 3.5 The Logic Probe
   - 3.6 Providing Logic Signals with Switches
     - 3.6.1 SPST Switches
     - 3.6.2 The SPST Switch Circuit
     - 3.6.3 Active HI/Active LO Signals
     - 3.6.4 Documentation of Switch Circuits

4. Logic Operations and Gates (4 hrs)
   - 4.1 Basic Logic Operations
   - 4.2 Logic Symbols for Real Devices
   - 4.3 Naming Gates
   - 4.4 Gate Duality
   - 4.5 Introduction to Digital ICs
   - 4.6 LEDs as Logic Indicators
     - 4.6.1 Basic LED Operation
     - 4.6.2 The 74LS244 Buffer
     - 4.6.3 Active HI/Active LO LED Circuits
   - 4.7 Hardware Options

5. Analysis of Combinatorial Circuits (6 hrs)
   - 5.1 Describing Logic Circuits Algebraically
   - 5.2 Evaluating Circuit Outputs
   - 5.3 Boolean Theorems
   - 5.4 The Boolean Sum-Of-Products Form
   - 5.5 Truth Tables from SOP Expressions
   - 5.6 Redrawing Circuits: Appropriate Use of Duals

5. Analysis of Combinatorial Circuits *(continued)*
   - 5.7 Fault Finding in Combinatorial Circuits
     - 5.7.1 Acceptable Voltage Levels (LSTTL)
     - 5.7.2 Common Faults
     - 5.7.3 A Systematic Approach

6. Common Circuit Configurations (2 hrs)
   - 6.1 Gating (Enable/Inhibit) Circuits
   - 6.2 Data Distributor (Steering) Circuits
   - 6.3 Encoders/Decoders
     - 6.3.1 Encoders
     - 6.3.2 Decoders
     - 6.3.3 Example: Decoding to a 7-Segment Display
     - 6.3.4 Decoding with PLDs

*** Exam (Tutorial, Mid-Term Test, Review of Test) (2 hrs)

7. Introduction to Logic IC Parameters (1 hr)
   - 7.1 Current: Capability vs. Demand
   - 7.2 Definitions: IC Voltage and Current Parameters
   - 7.3 Introduction to IC Specifications
   - 7.4 Application of IC Output Specifications

8. Sequential Logic Concepts (4 hrs)
   - 8.1 Introduction to Sequential Logic
   - 8.2 Clocks
     - 8.2.1 Basic Concepts
     - 8.2.2 IC Devices and Circuits
   - 8.3 One-Shots
     - 8.3.1 Basic Concepts
     - 8.3.2 IC One-Shots
   - 8.4 Flip-flops
     - 8.4.1 Basic Concepts
     - 8.4.2 RS Flip-flop (RS Latch)
     - 8.4.3 D Flip-flop
     - 8.4.4 Transparent D Flip-flop (D Latch)
     - 8.4.5 JK Flip-flop
     - 8.4.6 Switch Debounce
     - 8.4.7 Timing Parameters
     - 8.4.8 Example: A Simple Sequential Circuit

*** Exam (Tutorial, Mid-Term Test, Review of Test) (2 hrs)

9. Registers (1 hr)
   - 12.1 Flip-flop Data Storage and Transfer
   - 12.2 Register-to-Register Data Transfer
   - 12.3 Serial Load/Circulate Operations
   - 12.4 IC Registers

10. Counters (3 hrs)
   - 13.1 General Concepts
   - 13.2 Asynchronous Counters
   - 13.3 Synchronous Counters
   - 13.4 Cascaded Counters
   - 13.5 IC Counters

11. Digital Multiplexing (2 hrs)
   - 14.1 General Concepts
   - 14.2 Multiplexers
   - 14.3 Demultiplexers
   - 14.4 Multiplexed Displays
   - 14.5 Tristate and Open-Collector Logic

12. IEEE/ANSI Logic Symbols (1 hr)
   - 15.1 Introduction
   - 15.2 Symbol Attributes
   - 15.3 Examples

Review: (1 hr)

Total (33 hrs)

LABORATORY EXERCISES

Lab Period:

1. INTRODUCTION
- Introduction to ELEX 164 Lab requirements.
- Identification of ICs.
- Issue and checking of parts kits.

2. LOGIC LEVELS
- Setting up breadboard Vcc and ground rails
- Logic probes
- Providing logic levels with SPST switches

3. LOGIC GATES
- Operation of SSI Logic ICs

4. GATE DUALITY and LED CIRCUITS
- Use of alternate gate symbols
- Active HI and active LO LED circuits

5 COMBINATORIAL LOGIC CIRCUITS
- Analysis of combinatorial circuit operation
- Construction and testing of logic circuits
- Introduction to fault finding

6. FAULT FINDING (Combinatorial Logic)
- Application of fault finding techniques to combinatorial logic circuits

7. GATING CIRCUITS
- Operation of Gating (Enable/Inhibit) and Data Distributor (Steering) circuits

8. DECODERS
- Operation of a Decoder IC for a 7-Segment LED Display

9. FLIP-FLOPS
- Operation of RS, JK, D, and Transparent D flip-flops.
- Effect of switch bounce.

10. SEQUENTIAL LOGIC CIRCUITS
- Analysis of a simple sequential logic circuit
- Construction and testing of a sequential circuit
- Introduction to fault finding in sequential logic circuits

11. FAULT FINDING (Sequential Logic)
- Application of fault finding techniques to sequential logic circuits